28278

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Chen-Jung TSAI :

Serial No. 10/074,052 ✓ : Group Art Unit: 2827

Filed: February 14, 2002 : Examiner: Lourdes C. Cruz

For: SEMICONDUCTOR PACKAGING DEVICE AND MANUFACTURE THEREOF

Dear Sir:

Transmitted herewith is an Amendment in the above identified application.

☐ No additional fee is required.
☐ Small entity status of this application has been established .
☒ Also attached: Request for Approval of Drawing Revision

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	13	20	0	x $ 18 =	$ 0.00
Independent Claims	5	4	1	x $ 84 =	84.00
		If multiple claims newly presented, add $280.00			
		Fee for extension of time			
				TOTAL FEE DUE	**$84.00**

☒ A credit card authorization form in the amount of $84.00 is attached
☐ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 07-1337, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	**10/074,052**
Applicant	:	**TSAI ET AL.**
Filed	:	**February 14, 2003**
Title	:	**SEMICONDUCTOR PACKAGING DEVICE MANUFACTURE THEREOF**
Art Unit	:	**2827**
Examiner	:	**LOURDES C. CRUZ**
Docket No.	:	**4425-248**

Honorable Commissioner for Patents
P. O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

Sir:

In response to the Office Action of February 27, 2003, to which a response is due by May 27, 2003, please amend the above-identified application as follows:

In the Abstract:

Please replace the original abstract with the following rewritten paragraph:

--A semiconductor packaging device has a carrier having at least a cavity for fitting at least a chip. The chip has a back surface, an active surface with first bonding pads, and a sidewall connecting the back surface and the active surface. The back surface and the sidewall of the chip are affixed to the cavity and expose the active surface. A first insulating layer is coated on both the active surface and the carrier, and has first conductive holes therein. The first conductive holes are corresponding to first bonding pads. A multi-layer structure is on the first insulating layer, which has conductive layout lines, second conductive holes therein, a second insulating layer thereon and exposed ball pads in the second insulating layer. The first conductive holes are electrically connected with the conductive layout lines, the second conductive holes, and the exposed ball pads. A plurality of solder balls are affixed to the ball pads.--